REMARKS

After the foregoing Amendment, claims 1, 3-6, and 16 are currently pending in this application. Claims 2 and 7 have been canceled in the present reply without prejudice. Claims 1, 3, 4 and 16 are amended. Applicants submit that no new matter has been introduced into the application by these amendments.

Claim Rejections - 35 U.S.C. § 103

Claims 1, 4, 5, and 16 stand rejected under 35 U.S.C § 103(a) as being unpatentable over Nassiri-Toussi et al. (U.S. Ref. No. 7,194,011 B1, hereinafter "Nassiri") in view of Frigon (U.S. Ref. No. 7,173,992 B2, hereinafter "Frigon") and Yamaguchi (U.S. Ref. No. 2003/0119444 A1, hereinafter "Yamaguchi"). The Applicants respectfully disagree.

With respect claims 1 and 16, Nassiri discloses a peak detector that may disregard peaks that are not greater than a threshold. Of the remaining peaks, the peak detector disclosed in Nassiri identifies the highest peak and its sample position in cyclic buffer becomes a maximum index value. The peak value outputs from the peak detector disclosed in Nassiri and the corresponding index values are used by a slot timing calculation block to generate the slot timing information that is used by a secondary search stage.

There is no disclosure, teaching, or suggestion in the Nassiri reference of receiving a SCH signal that has been transmitted in a predetermined timeslot of a system time frame and includes a primary synchronization code (PSC) transmitted in the timeslot at a predetermined chip offset wherein the decoding includes determining a t_{offset} at which the selected SCH is transmitted.

Nassiri further discloses a matched filter that receives a stream of 8-bit in-phase samples at twice the chip rate and a stream of 8-bit quadrature samples at twice the chip rate. The matched filter in Nassiri detects the unmodulated complex-valued 256-chip code word in the primary synchronization channel (PSCH) channel signal. The matched filter in Nassiri contains two select every 32nd sample blocks. The select every 32nd sample blocks read out every 32nd entry and passes the eight samples to an 8-tap complex correlator from processing. The select every 32nd sample blocks then decrements and grabs another group of 8 entries that are spaced 32 entries apart.

There is no disclosure, teaching, or suggestion in the Nassiri reference of identifying whether the chip location of the PSC sequence was derived from an even sample or an odd sample where the PSC sequence is identified by processing a wireless communication signal at twice the chip rate.

With respect claims 1 and 16, Frigon discloses a selection diversity receiver that employs M parallel diversity branches. Each diversity branch disclosed in

Frigon receives a time dependent signed S_m (t). Frigon discloses that in a selection diversity receiver the signal of the diversity branch with the highest instantaneous signal to noise ration (SNR) is selected and inputted into a slicer.

There is no disclosure, teaching, or suggestion in the Frigon reference of receiving a SCH signal that has been transmitted in a predetermined timeslot of a system time frame and includes a primary synchronization code (PSC) transmitted in the timeslot at a predetermined chip offset wherein the decoding includes determining a t_{offset} at which the selected SCH is transmitted. Further, there is no disclosure, teaching, or suggestion in the Frigon reference of identifying whether the chip location of the PSC sequence was derived from an even sample or an odd sample where the PSC sequence is identified by processing a wireless communication signal at twice the chip rate.

Accordingly, the Frigon reference fails to cure the deficiencies of the Nassiri reference.

With respect claims 1 and 16, Yamaguchi discloses the steps of a mobile user detecting in the SCH a sequence of repeats of a quadrature phase-shift keying (QPSK) symbol without scrambling and spread with a PSC. As disclosed in Yamaguchi, the SCH is the first 256 chips in each 2560 chip slot. The detection in Yamaguchi is performed by a filter matched to the PSC.

There is no disclosure, teaching, or suggestion in the Yamaguchi reference of a receiving a SCH signal that has been transmitted in a predetermined timeslot of a system time frame and includes a primary synchronization code (PSC) transmitted in the timeslot at a predetermined chip offset wherein the decoding includes determining a t_{offset} at which the selected SCH is transmitted. Further, there is no disclosure, teaching, or suggestion in the Yamaguchi reference of identifying whether the chip location of the PSC sequence was derived from an even sample or an odd sample where the PSC sequence is identified by processing a wireless communication signal at twice the chip rate.

Accordingly, the Yamaguchi reference fails to cure the deficiencies of the Nassiri and the Frigon references.

Therefore, amended independent claims 1 and 16 are patentable over the Nassiri, Frigon and Yamaguchi references, whether taken alone or in any combination with one another.

Claims 4 and 5 are dependent, either directly or indirectly, upon amended patentable independent claim 1 and are therefore patentable for at least the same reasons as amended patentable independent claim 1.

Based on the arguments presented above, withdrawal of the 35 U.S.C. 103(a) rejection of claims 1, 4, 5, and 16 is respectfully requested.

Conclusion

If the Examiner believes that any additional minor formal matters need to be addressed in order to place this application in condition for allowance, or that a telephonic interview will help to materially advance the prosecution of this application, the Examiner is invited to contact the undersigned by telephone at the Examiner's convenience.

In view of the foregoing amendment and remarks, Applicants respectfully submit that the present application is in condition for allowance and a notice to that effect is respectfully requested.

Respectfully submitted,

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